

DETAILED ACTION***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biard US 4,661,726 (Biard).

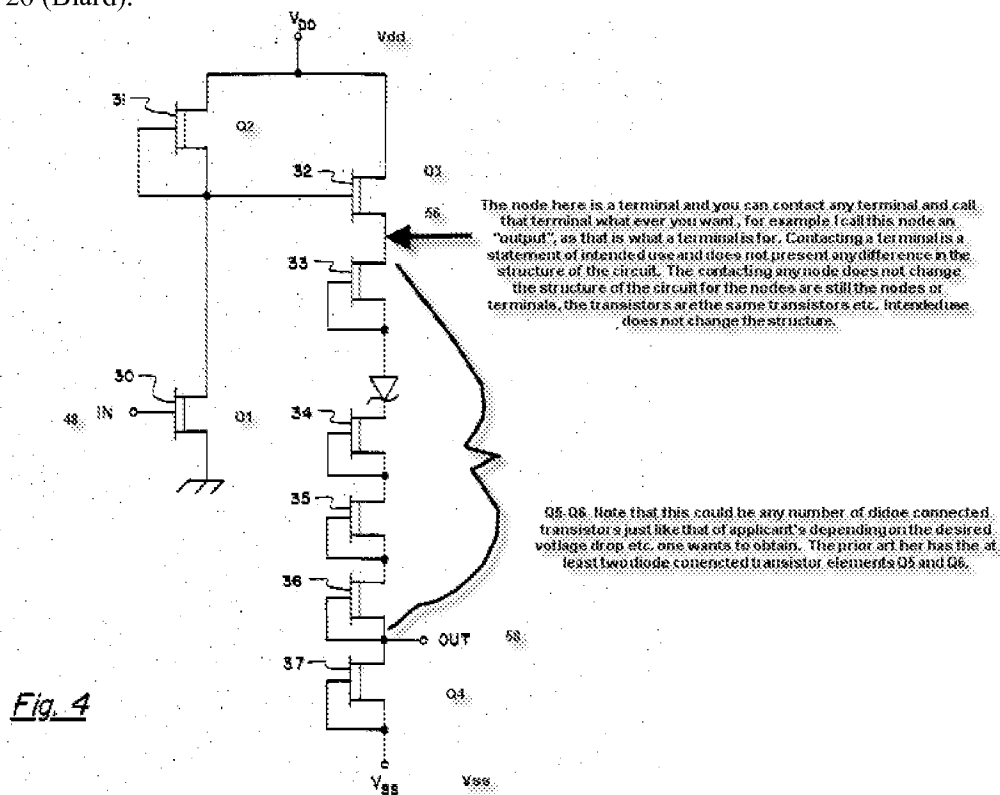


Figure 4 of Biard.

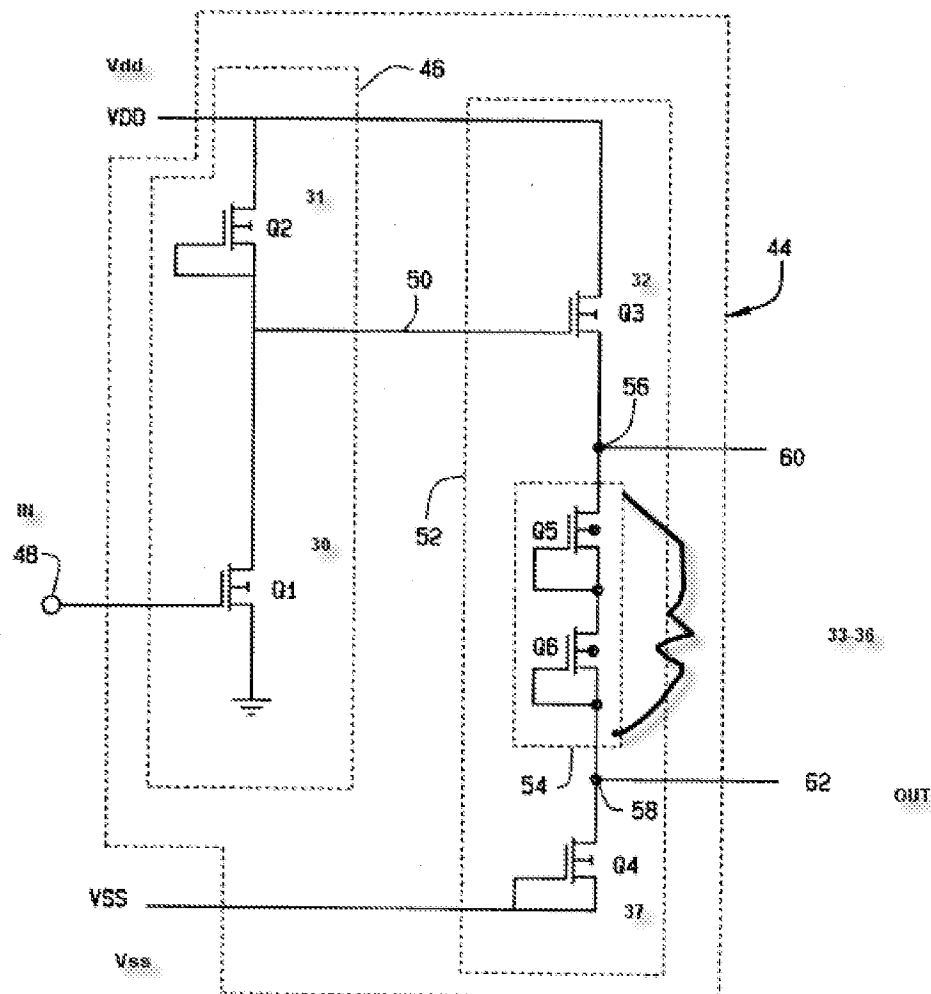


FIG. 2

Figure 2 of the instant application.

At least Figure 4 and the relevant text of Biard discloses a buffered field effect transistor. Rather than go through a long written description of how the prior art reads on applicant's structure here, the written description is presented in the reproduction of Figure 4 of Biard and Figure 2 of applicant's invention reproduced above.

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Biard is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. However, NMOS and PMOS depletion mode MOSFETs are conventional forms of depletion mode MOSFETs. The examiner still does not see any dispute of the well known nature of these elements. Biard also does not exclude the use of NMOS depletion mode MOSFETs. The only logical conclusion is that one could use either one. This is like forming a circuit just from PMOS transistors and then taking that circuit and form it from NMOS transistors. This is well known to have been obvious to one of ordinary skill in the art. One would have to change the voltage to activate a PMOS over and NMOS but this is all well within the level of routine skill in the art. This is just a well known fact. In fact given the polarity of the voltage sources being the same between the Biard reference and Figure 2 of the instant application it is a safe assumption that the Biard reference actually prefers or uses depletion mode NMOS transistors.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize depletion and only depletion mode NMOS transistors in the circuit of Biard because as the Biard reference is silent on the exact type of depletion mode MOS transistors used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode MOSFET such as the NMOS depletion mode MOSFET.

Response to Arguments

Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection. However it is clear that applicant believes that the statements on how to use the circuit will overcome the prior art. The examiner respectfully disagrees.

As recited in the response and office action of January 1, 2008 the examiner stated that the structure of a NMOS depletion mode transistor just would not make for a patentable distinction over the Baird reference is very specific that depletion mode FETs are to be used and there are only two types i.e. PMOS or NMOS. Baird just does not exclude NMOS types and is inclusive of both types. This choice of types is definitely obvious at the very least. The examiner while could not allow the claimed invention on this ground because as stated and explained above a NMOS is a well known type of depletion mode FET and the use of such would result in the circuit of Baird operating in a predictable manner. In fact the examiner contends that Baird even suggests this as Baird just does not exclude the conventional NMOS depletion mode type, however, at the very least applicant argued structure. MPEP 2114 clearly states that "while features of an apparatus may be recited either structurally or functionally, claims drawn to an apparatus must be distinguished from the prior art in terms of structure rather than function". In re

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Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). In the Schreiber case the prior art to funnel was viewed as anticipating the funnel structure of the application even though the funnel of the prior art did not recite the functional “popcorn” aspects. The deciding fact was whether that structure of the prior art was capable of providing the function which it was.

In response to applicant’s arguments the examiner will discuss in detail two of the statements added to the claims. This should make it clear that similar “statements” in the claims fails for similar reasons.

1.) The present claims dated 3-24-2008 states that the second node "is configured to transmit a chopping signal to a first chopping circuit". Applicant is again reminded that the current RCE is directed to the subcombination and not the subcombination of the 09/682,863. This was a result of the restriction in the 09/682,863 application. The term is “configured to” does not mean that the second node in this case must be connected, i.e. has to be connected to the first chopping circuit. If it did then this claim 26 and claims like that contain this language would be directed to the non-elected invention as that would be the combination. This is truly more of a statement of intended use. So as dictated above by MPEP 2114 and In re Schreiber above the examiner must ask what is the structural difference in the node of the invention compared to that of the prior art? and is there a structural difference in this node of the invention compared to that of the prior art? There must be no ambiguity as to what the structural difference is.

2.)As to another issue of the presently amended claims, the presently amended claims recites: "a clock input signal received at the inverter stage input" and this causes the chopping signal to be formed via the claimed circuit structure. The claims does not say that a clock source i.e. structure is connected to the level shifting/inverter stage structure. Again if it had then claims that contain this would be directed to the non-elected invention. Again this is more directed toward intended use. And again the examiner must ask what is the structural difference in the claimed circuit structure compared to that of the prior art? Again there must be no ambiguity as to what the structural difference is.

There must be no ambiguity as to what the structural difference is. This is “because claims delineate the patentee’s right to exclude, the patent statute requires that the scope of the claims be sufficiently definite to inform the public of the bounds of the protected invention, i.e. what subject matter is covered by the exclusive rights of the patent. Otherwise competitors cannot avoid infringement,

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defeating the public notice function of patent claims.” (Halliburton Energy Services, Inc. v M-I LLC (Fed. Cir. 2007-1149, 1/25/2008). The Halliburton decision goes on to state: “It is highly desirable that patent examiners demand that applicants resolve the ambiguity in the patent claims so that the patent can be amended during prosecution rather than attempting to resolve the ambiguity in litigation.”. The Halliburton decision also goes on to show that a claim where the inventor is painstaking when he recites what has already been seen, and then uses conveniently functional language at the exact point of novelty can render a claim(s) indefinite. Halliburton cites two cases with respect to this last issue namely General Electric, 304 U.S. at 371 and United Carbon, 317 U.S. at 234.

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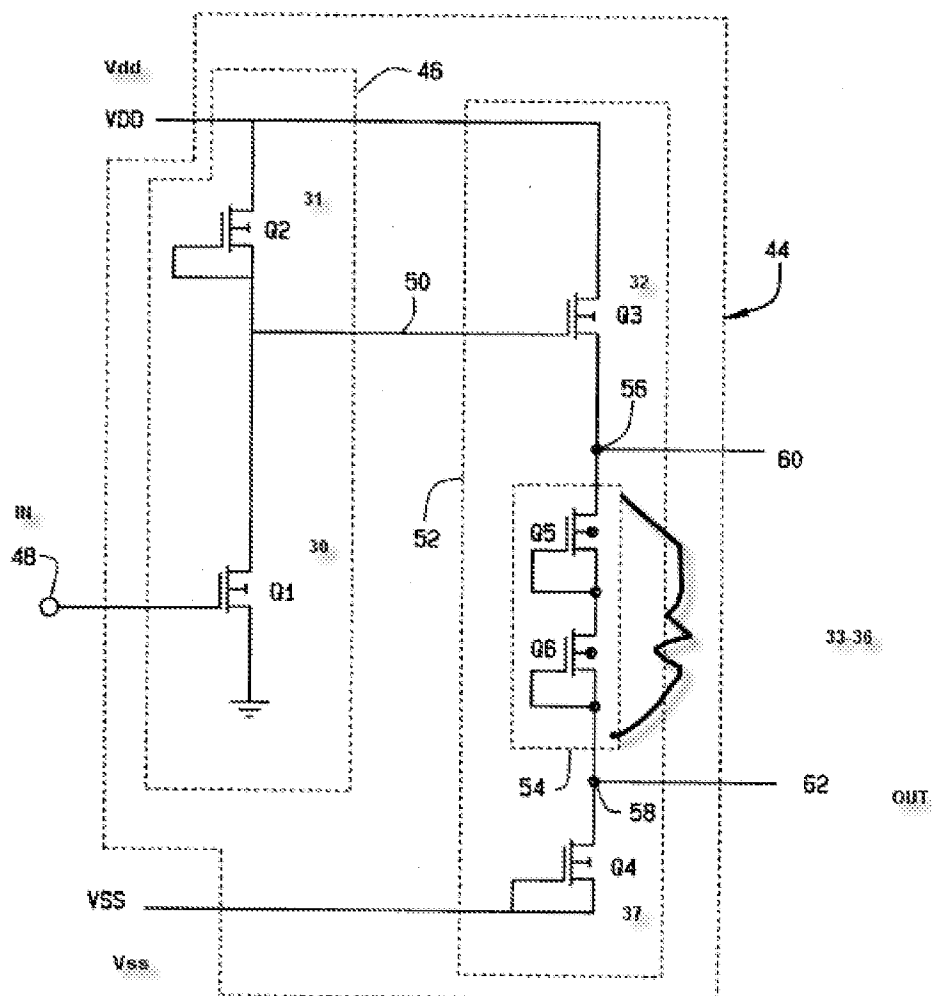


FIG. 2

Figure 2 of the instant application.

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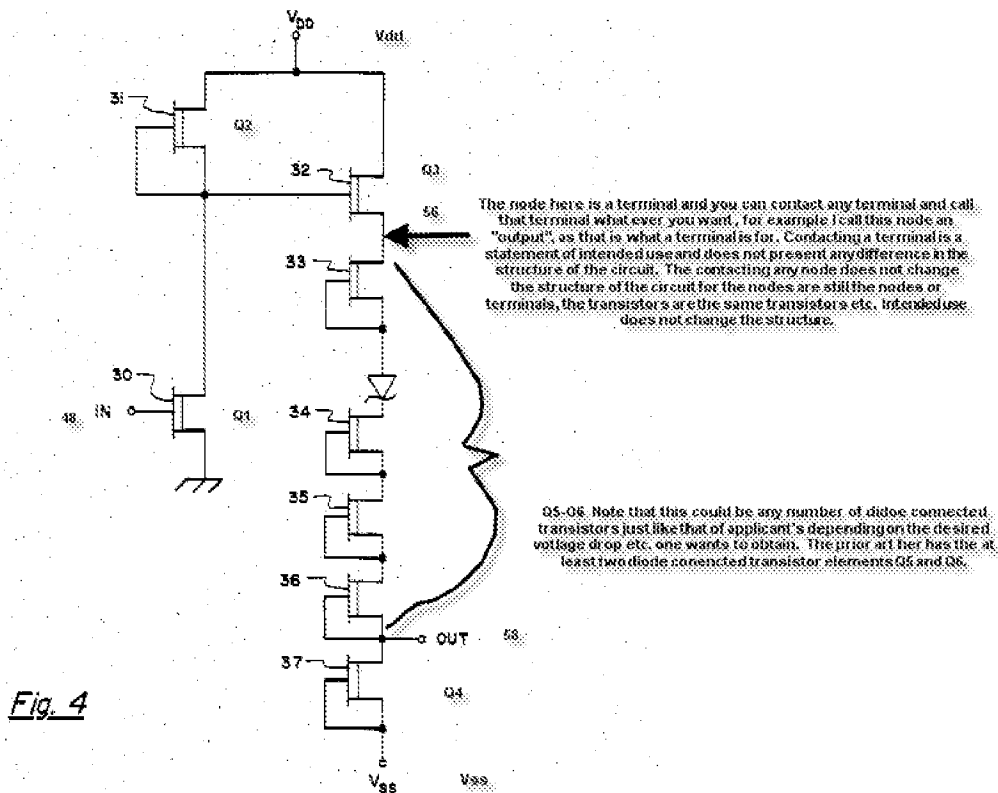


Fig. 4

Figure 4 of Biard.

So let's try to answer the question of what is the structural difference, if there is one. With respect to issue 1.) A node is a point of contact or (2) (network)(junction point)(branch point). A terminal of any branch or a network or a terminal common to two or more branches of a network. Of course a terminal is a point in a circuit where one can make contact with. The examiner has copied Figure 4 of Biard and Figure 2 of the instant application where on page 3 of the specification applicant describes Figure 2 of the instant application as "a schematic diagram of one embodiment of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifter/inverter that is suitable for use in the operational amplifier represented in Figure 1 (emphasis added) See even here even applicant distinguishes between the structure of the level shifter/inverter and the use i.e. where applicant would like to connected the structure with. Applicant recognizes the difference between the structure of the level shifter/inverter and the use of the level shifter/inverter, i.e. where applicant intends to connect the circuit to and what voltages/currents applicant intends to apply. So does the nodes of Figure 2 of the instant application have a different metal arrangement that makes up these nodes compared to the node of the Biard reference? No. The node structure is not recited by the Figures or the specification of the instant

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application. Again a node is a terminal and as with any terminal one can connect thereto. Is there anything that prevents a connection to any of the nodes, i.e. terminals in the prior art circuit of Biard? No. One can make contact with any node one desires. Making contact to the circuit is how one intends to use the circuit and it is not the circuit itself. This should make it pretty clear that what the structural difference is here is very ambiguous at best.

With respect to issue 2.), here applicant says that a clock signal is "received" at the input of the inverter stage. Figure 2 of the instant application does not show a clock signal as "received" and applicant is very clear as indicated above and on page 3 of the specification that the potentials from other circuits that are to be applied to the circuit of Figure 2 are absolutely not part of the level shifting/inverter stage but are part of how applicant intends to use the circuit and applicant uses the word "use". A potential difference, i.e. voltage is not a structure. So let's try to answer the question of what is the structural difference? Is the input node made of a different material than the prior art? No. Is the input node somehow changed structurally by applying a clock signal. The examiner would have to say no because there is not indication of such in the original disclosure. In fact as noted above there is not disclosure as to the composition of the nodes, i.e. terminals, of the circuit. Ok, so is there some other structural difference? The examiner does not find any, the Q1 of the instant application is the same as 30 of the prior art etc. Note that the examiner has indicated the similar structures on the above reproductions of the Figure 2 of the instant application and the Figure 4 of the prior art. From all indications the circuit of Biard must function the same as that of applicants when the various voltages and loads are connected to the circuit like that of applicant's circuit. Again this should make it pretty clear that what the structural difference is here is very ambiguous at best.

The ambiguous nature of what the structural difference is just does not serve the public interest and it would not be in litigation where the ambiguity is resolved as recited by Halliburton above. The examiner has and still attempts to resolve the ambiguity here. All indication is that the prior art structure when connected i.e. used in the manner as intended will function as claimed. Again the examiner refers to the In re Schreiber case law above. If the funnel structure of the prior art which described oil being applied would anticipate the funnel structure claimed since the funnel structure of the prior art is fully capable of performing the function when one would apply popcorn to that funnel. You apply the same voltages and output at the nodes the prior art structure of Biard from all indication will perform the same. Truly the circuits of the Biard and that of applicant's Figure 2 are very much the same structure and because of this the examiner just does not know of any way or structure applicant can claim to overcome the prior art.

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Another way of looking at the issues in the present case, let's say we have a 10Ohm $\frac{1}{2}$ watt carbon resistor structure i.e. circuit that exists in the prior art. Let's say that applicant claims a resistor circuit of 10 Ohms, $\frac{1}{2}$ Watt and made of carbon and then uses functional language at the exact point of "novelty" such as having a first node of the resistor configured to "receive" or actually receives a 100,000 volt peak to peak 10 Hz clock signal and that the other node of the resistor configured to transmit this "chopping signal" signal produced at this "other node" directly connected to ground until the function of a fuse is obtain, i.e. the resistor blows and blows rather quickly. Radio Shack let's say is the prior art that shows a 10Ohm $\frac{1}{2}$ watt carbon resistor, i.e. circuit. If you take the Radio Shack circuit, i.e. the 10Ohm, $\frac{1}{2}$ Watt carbon resistor and connect in the manner as applicant intends to use this circuit, will the prior art Radio Shack circuit function as claimed? Yes, because no 10 Ohm $\frac{1}{2}$ Watt resistor can withstand a 100,000 volt peak to peak 10 Hz source.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker, can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MBS
May 11, 2008

/Michael B. Shingleton/
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Primary Examiner
Group Art Unit 2815

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